

Figure 1 shows a schematic diagram of a differential amplifier circuit. The circuit is powered by V_{DD} and V_{SS} . It features a differential pair of NMOS transistors (M1, M2) with a PMOS load (M3, M4). The output is taken from the differential output nodes (M19, M20). The circuit includes various biasing and matching components, such as current sources (M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18) and resistors (M19, M20). The output voltage is labeled V_{OUT} . The input voltage is labeled V_{IN} . The output voltage is labeled V_{OUT} . The circuit is labeled "Matched" at two locations.

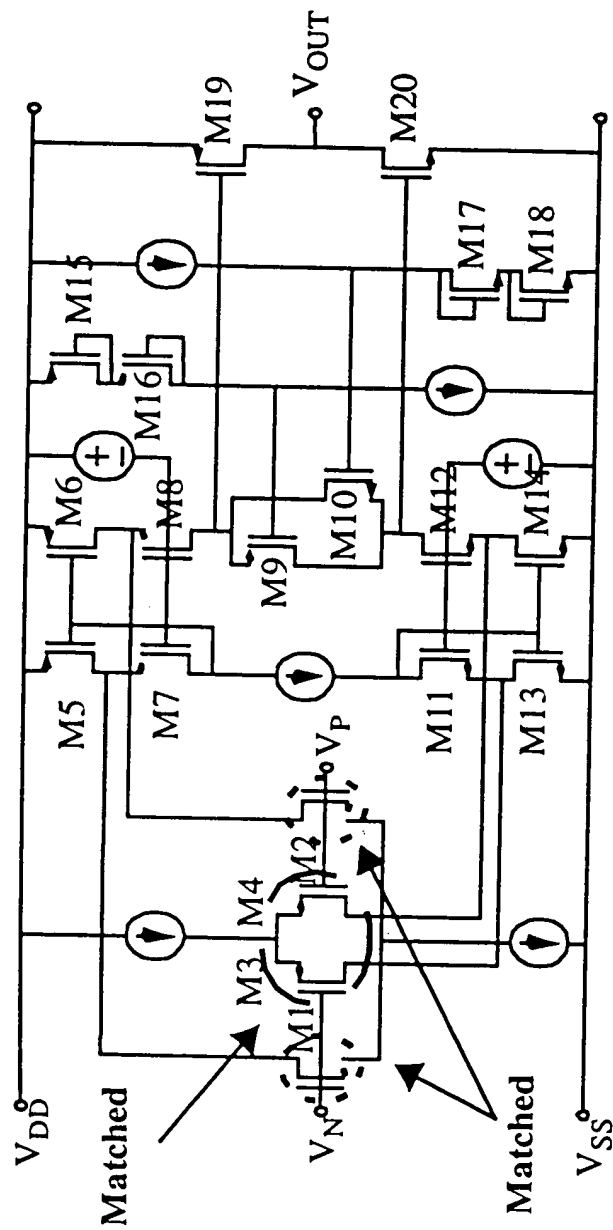


FIGURE 1

Impact of mismatch on offset voltage of an opamp

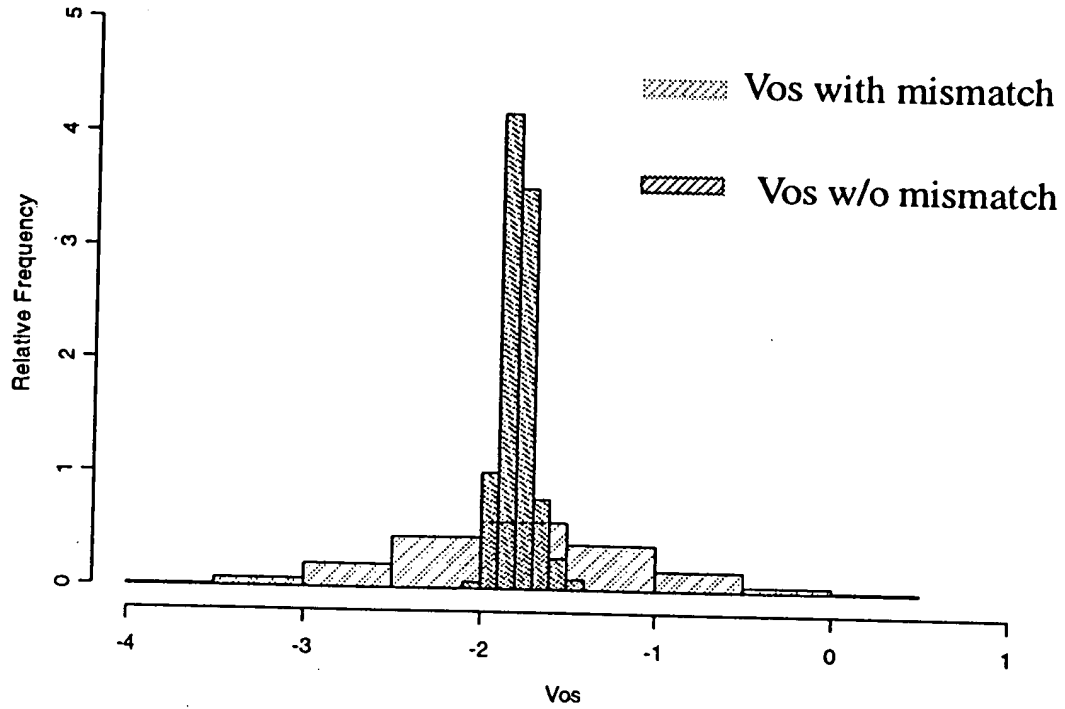


FIGURE 2

Std dev of DNL for a 8 bit DAC

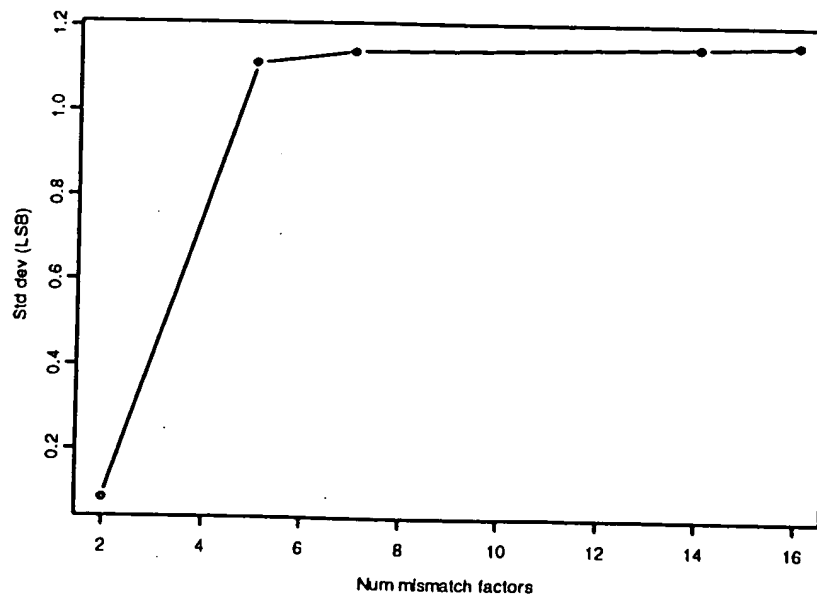


FIGURE 4

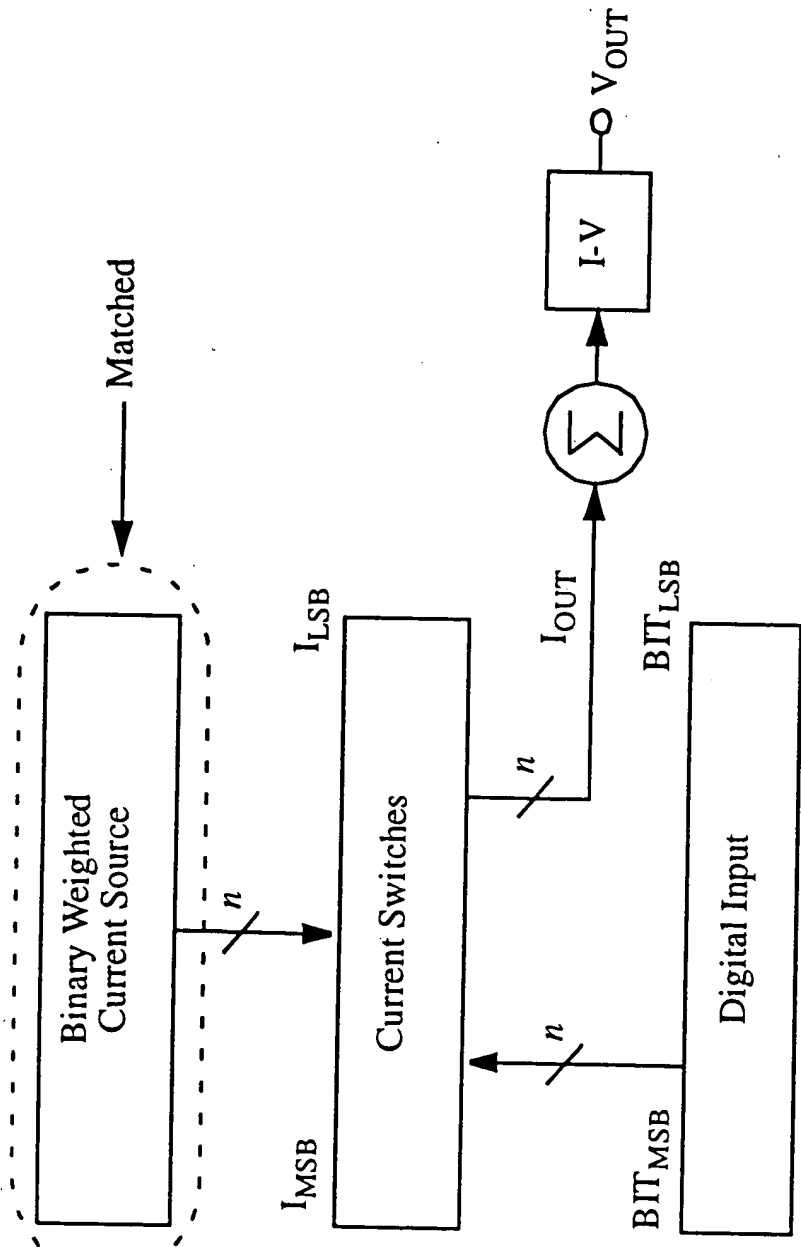


FIGURE 3